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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,380	10/31/2003	Stephen M. Trimberger	X-1435 US	1825

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
MORAN, RANDAL D	

ART UNIT	PAPER NUMBER
2435	

MAIL DATE	DELIVERY MODE
11/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/714,380	TRIMBERGER, STEPHEN M.	
	Examiner	Art Unit	
	RANDAL D. MORAN	2435	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 12 November 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-3 and 6-16*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

/Kimyen Vu/
Supervisory Patent Examiner, Art Unit 2435

/R. D. M./
Examiner, Art Unit 2435

Continuation of 11. does NOT place the application in condition for allowance because: Aplicant's arguments have been fully considered but are not persuasive.

Regarding Claim 1, Applicant's arguments have been fully considered but are not persuasive. With respect to applicant's argument that the combination fails to teach "the decryptor is a software decryptor stored in a memory and executed by the microcontroller," applicant is directed to Pang- column 13- lines 37-56, Fig. 8 and Lesea- column 4- lines 12-25, Fig. 1. Pang discloses:

> "At step 82, two words (64 bits) of encrypted configuration data are loaded into decryptor 24. At step 83 the addressed key is loaded into decryptor 24. In one embodiment, a 64-bit number is loaded into decryptor 24. This 64-bit number includes a 56-bit key, two bits that indicate whether it is the first, middle, last, or only key, and some other bits that may be unused, used for parity, or used for another purpose. In another embodiment, the 64-bit key data includes a single bit that indicates whether it is or is not the last key. In yet another embodiment, the 64-bit key data includes an address for the next key so the keys don't need to be used in sequential order. In another embodiment, extra bits are not present and the key data uses less than 64 bits. In yet another embodiment, the bitstream rather than the key indicates how many keys are to be used, but this is believed to be less secure because an attacker can see how many keys are used and perform a single key attack, breaking one key at a time, whereas using the keys to indicate how many keys are to be used does not give this information to an attacker."

Lesea discloses:

> "As illustrated in the expanded portion at the bottom of FIG. 1, corner block 5 includes a processor 9, an on-chip oscillator 10, an amount of non-volatile memory 11 (for example, ROM or FLASH memory), an amount of random-access-memory (RAM) 12, decoding circuitry 13, interface logic 14 to interface with selected IOB terminals during configuration, and interface logic 15 to write to and read from the configuration memory cells of the remaining IOBs 2, CLBs 7 and the programmable interconnect structure 8."

Lesea teaches a processor (i.e. microcontroller), an amount of non-volatile memory, an amount of random-access memory (i.e. memory to store a decryptor). Pang teaches loading bits into a decryptor as well as a key management system to determine adddresses for the next key (i.e. software to control the decryptor and keys). Therefore, the combination of Pang and Lesea discloses that the decryptor is a software decryptor stored in a memory and executed by the microcontroller.

With respect to applicant's argument that the combination fails to teach "selectively enables access to the key storage register by allowing the microcontroller access when a program counter of the microcontroller specifies an address within an address range corresponding to the software decyptor within memory," applicant is dieected to Pang- column 20- lines 27-53, Lesea- column 6- lines 40-53. As disclosed by the applicant, the program counter contains the address of the current or next instruction to be implemented. Therefore, the program counter of the combination is required to contain a read instruction containing the address of the decryptor if the decryptor is to be used. This is a requirement of every system. The decryptor is contained within memory and when the decryptor is accessed, it's location in memory is read out using the program counter.

Regarding Claim 19, Applicant's arguments have been fully considered but are not persuasive. With respect to applicant's argument that the combination fails to teach "uses specified addresses of the non-volatile memory by limiting access to minimum and maximum ROM memory addresses using the microcontroller program counter," applicant is directed to Kuranaga- column 6- lines 56-67. As decribed above, the addresses being read must be within the range of the decryptor to access the key storage register. If the addresses within the program counter are not within the address range of the decryptor, it is impossible to read from the key storage register.